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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/727,786

12/04/2003

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EXAMINER

PETERSON, CHRISTOPHER K

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/727,786	Applicant(s) JUNG, DUCK YOUNG	
	Examiner CHRISTOPHER K. PETERSON	Art Unit 2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 February 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-5,7 and 8 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3-5,7 and 8 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 2/4/2008 was filed after the mailing date of the non-final rejection on 11/27/2007. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Response to Arguments

2. Applicant's arguments, see Remarks (pages 5 – 8), filed 2/27/2008, with respect to the rejection(s) of claim(s) 1, 3 – 5, 7, and 8 under 35 USC 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Fujimori (Japanese Patent # 6-165047) and Matsushima (US Patent Pub. 2003/0016299).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Fujimori (Japanese Patent # 6-165047).

As to claim 1, Fujimori (Fig. 1) teaches an image signal processing system comprising:

- an image sensor (CCD 2) for receiving an image of a subject in a light form under the control of a shutter control signal (shutter speed) to generate analog signals (Para 19). Fujimori teaches the shutter speed for the CCD (2) is determined by the system controller (10) (Para 46)
- a variable gain amplifier (automatic gain control circuitry (AGC) 3) for amplifying output signals of the image sensor (CCD 2) under the control of a gain control signal to maximize dispersion of the analog signals (Para 19). Fujimori teaches the AGC is a gain variable amplifying means (Para 19).
- a first A/D converter (A/D 4) for receiving the output signals of the variable gain amplifier (3) and converting the received output signals into digital signals (Para 19);
- a second A/D converter (A/D 7) for receiving the output signals of the image sensor (2) and converting the received output signals into the digital signals (Para 20); and
- an image data processor (system controller 10) for receiving the output signals of the first A/D converter (4) and the output signals of the second A/D converter (7) to find a movement value (motion vector), generating the

gain control signal (variable control of AGC) and the shutter control signal (shutter speed), and providing the generated shutter control signal to the image sensor (2) (Para 46 and 47).

- wherein the shutter control signal (shutter speed) is generated by the output signals of the second A/D converter (Para 46). Fujimori teaches that the shutter speed is determined by the luminance level data that supplied from the second A/D (7).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimori (Japanese Patent # 6-165047) in view of Matsushima (US Patent Pub. # 2003/0016299).

As to claim 5, this claim differs from claim 1 only in that the limitation “a direct current offset controller” is additionally recited. The direct current offset controller is connected between the CCD and the variable control amplifier. The Matsushima reference teaches a clamp / CDS (7) which is connected to the output of the CCD (6) and the input of the auto-gain control (AGC (8)). Matsushima teaches a direct current

offset controller (clamp / CDS 7) for controlling direct current offsets of output signals of the image sensor (CCD 6) under the control of an offset control signal (clamp level) (Para 29). Matsushima teaches that the clamp level can be changed by the microcomputer (16) (Para 29). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided a direct current offset controller as taught by Matsushima to the image pickup device of Fujimori, because a clamp / CDS removes reset noise from the image data and provides an enhanced image quality.

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimori (Japanese Patent # 6-165047) in view of Shiga (US Patent Pub # 2005/0062874).

As to claim 3, Fujimori teaches the limitation "variable gain amplifier". Fujimori does not teach a variable gain amplifier is a sample-and-hold amplifier architecture. Shiga (see fig. 1) teaches a variable gain amplifier (4) as a sample-and-hold amplifier architecture. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided a variable gain amplifier with a sample-and-hold amplifier architecture taught by Shiga to the variable gain amplifier of Fujimori in view of Matsushima, because the use of a sample and hold / gain control circuit is advantageous in that it does not give rise to such deterioration of a signal or decrease of the information amount of image data (Para 0105 of Shiga).

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimori (Japanese Patent # 6-165047) in view of Matsushima (US Patent Pub. 2003/0016299), and further in view of Shiga (US Patent Pub # 2005/0062874).

As to claim 7, Fujimori in view of Matsushima teach the limitation “variable gain amplifier“. Fujimori in view of Matsushima do not teach a variable gain amplifier is a sample-and-hold amplifier architecture. Shiga (see fig. 1) teaches a variable gain amplifier (4) as a sample-and-hold amplifier architecture. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided a variable gain amplifier with a sample-and-hold amplifier architecture taught by Shiga to the variable gain amplifier of Fujimori in view of Matsushima, because the use of a sample and hold / gain control circuit is advantageous in that it does not give rise to such deterioration of a signal or decrease of the information amount of image data (Para 0105 of Shiga).

9. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimori (Japanese Patent # 6-165047) in view of Nagata (US Patent # 6,366,228).

As to claim 4, Fujimori teaches the limitation “A/D converter“. Fujimori does not teach an A/D converter is configured of a plurality of analog comparators. Nagata (see fig. 8) teaches an A/D converter configured of a plurality of analog comparators (CMP1 – 4) (Col. 12, lines 24 – 53). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided an A/D converter with a plurality of analog comparators taught by Nagata to the A/D converter of Fujimori,

because the use of analog comparators reduces the manufacturing cost and power (Col. 18, lines 43 - 55).

10. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimori (Japanese Patent # 6-165047) in view of Matsushima (US Patent Pub. 2003/0016299) and further in view of Nagata (US Patent # 6,366,228).

As to claim 8, Fujimori in view of Matsushima teach the limitation "A/D converter". Fujimori in view of Matsushima do not teach an A/D converter is configured of a plurality of analog comparators. Nagata (see fig. 8) teaches an A/D converter configured of a plurality of analog comparators (CMP1 – 4) (Col. 12, lines 24 – 53). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided an A/D converter with a plurality of analog comparators taught by Nagata to the A/D converter of Fujimori in view of Matsushima, because the use of analog comparators reduces the manufacturing cost and power (Col. 18, lines 43 - 55).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Araki (US Patent # 5,278,659) cites a shutter speed control circuit for an image pick-up apparatus. Araki teaches an exposure control apparatus for a video camera in which exposure can be controlled at high accuracy even when the shutter speed is very high.

Inquiries

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTOPHER K. PETERSON whose telephone number is (571)270-1704. The examiner can normally be reached on Monday - Friday 6:30 - 4:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, NgocYen Vu can be reached on 571-272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CKP
15 May 2008

***/Ngoc-Yen T. VU/
Supervisory Patent Examiner, Art Unit 2622***